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15/690,698	08/30/2017	Greg J. MAYNARD	JRL-4010-410	8464

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EXAMINER
ALLADIN, AMBREEN A

ART UNIT	PAPER NUMBER
3693	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No. 15/690,698	Applicant(s) MAYNARD, Greg J.	
	Examiner AMBREEN A ALLADIN	Art Unit 3693	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 06/19/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. This action is in reply to the Request for Reconsideration dated June 19, 2020.

2. **Claims 1-20** are currently pending and have been examined.

3. **Claims 3, 5, 7, 10, 12, 17 and 19** have been amended.

4. This application is a Continuation of Application 13/834,843, now abandoned. The instant claims are drawn more narrowly than the claims of the previous application and thus at this time there is no prior art being asserted.

Notice of Pre-AIA or AIA Status

5. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. **Claims 1-20** are rejected under 35 U.S.C. § 101 because the claimed invention is directed to an abstract idea without significantly more.

The independent claims recite substantially similar claims as to a system, method and a FPGA circuit reciting a matcher to store an order book that stores pending orders configured to receive a first order electronic message for a first instrument and perform a matching performance on the first order electronic message, a gateway to receive and route the first order electronic message for matching; receive a first mass quote message associated with a first client that includes a plurality of individual quote electronic messages that are bundled into the first mass quote electronic message, each one including a price value for one of a plurality of different instrument identifiers included with a respective one of the plurality of individual quote electronic messages; route the mass quote message to the FPGA circuit without first involving the matcher and reconfigurable firmware logic circuitry configured to receive the mass quote electronic message, parse each one of the plurality of individual quote messages of the mass quote electronic message and store data for each one in a data structure where each of the plurality of individual quote electronic messages are organized according to both the instrument

identifier of a corresponding electronic message and a first client identifier, receive away market feed electronic messages where each message includes a price value and corresponding instrument identifier where each of the away market feed electronic messages are received by the FPGA without first being routed through the matcher or gateway, update the data structure based on reception of the away market feed messages and deliver in response to a query sent as part of the matching process information stored in the data structure regarding the first instrument which includes data based on away market feed electronic messages for the first instrument and data based on the individual quote electronic messages for the first instrument that were part of the at least one received mass quote electronic message.

The series of steps recited describe using a distributed computing to receive orders, send orders, parse orders, match orders, update data and deliver information regarding the match which is a fundamental economic practice and a commercial or legal interaction and thus grouped as certain methods of organizing human activity which is an abstract idea.

ANALYSIS:

STEP 1:

Does the claimed invention fall within one of the four statutory categories of invention (process, machine, manufacture or composition matter?

Yes and No. The claimed invention recite substantially similar claims as to a system, method and a FPGA circuit reciting a matcher to store an order book that stores pending orders configured to receive a first order electronic message for a first instrument and perform a matching performance on the first order electronic message, a gateway to receive and route the first order electronic message for matching; receive a first mass quote message associated with a first client that includes a plurality of individual quote electronic messages that are bundled into the first mass quote electronic message, each one including a price value for one of a plurality of different instrument identifiers included with a respective one of the plurality of individual quote electronic messages; route the mass quote message to the FPGA circuit without first involving the matcher and reconfigurable firmware logic circuitry configured to receive the mass quote electronic message, parse each one of the plurality of individual quote messages of the mass quote electronic message and store data for each one in a data structure where each of the plurality of individual quote electronic messages are organized according to both the instrument identifier of a corresponding electronic message and a first client identifier, receive away market feed electronic messages where each message includes a price value and corresponding

instrument identifier where each of the away market feed electronic messages are received by the FPGA without first being routed through the matcher or gateway, update the data structure based on reception of the away market feed messages and deliver in response to a query sent as part of the matching process information stored in the data structure regarding the first instrument which includes data based on away market feed electronic messages for the first instrument and data based on the individual quote electronic messages for the first instrument that were part of the at least one received mass quote electronic message. Currently the FPGA circuit claim has a separate rejection as being non-statutory (as shown below) but Examiner assumes Applicant will rectify the claims to properly claim the invention as within statutory categories.

STEP 2A:

Prong One: Does the Claim Recite A Judicial Exception (An Abstract Idea, Law of Nature or Natural Phenomenon)? (If Yes, Proceed to Prong Two, If No, the claim is not directed to a judicial exception and qualifies as subject matter patent eligible material)

As recited above, the series of steps recited describe using a distributed computing to receive orders, send orders, parse orders, match orders, update data and deliver information regarding the match which is a fundamental economic practice and a commercial or legal interaction and thus grouped as certain methods of organizing human activity which is an abstract idea.

Claim 1 recites a matcher server including a processing system with at least one hardware processor, a memory, a FPGA circuit that comprises reconfigurable firmware logic circuitry and memory. Claim 8 recites a matcher server with a memory and a FPGA circuit. Claim 15 recites a FPGA circuit with a memory, a matcher server, reconfigurable firmware logic circuitry and memory. The claims are just applying generic computer components to the recited abstract limitations. The reconfigurable firmware logic circuitry appears to be software. (*Step 2A – Prong 1; Yes, the claims are abstract)*

Prong Two: Does the Claim Recite Additional Elements That Integrate The Judicial Exception Into A Practical Application of the Exception? (If Yes, the claim is not directed to a judicial exception and qualifies as subject matter patent eligible material. If No, Proceed to Step 2B)

The claims do not include additional elements that integrate the judicial exception into a practical application of the exception because the claims do not provide improvements to another technology or technical field, improvements to the functioning of the computer itself, are not applying

or using a judicial exception to effect a particular treatment or prophylaxis for a disease or medical condition, are not applying the judicial exception with, or by use of a particular machine, are not effecting a transformation or reduction of a particular article to a different state or thing, and are not applying the judicial exception in some other meaningful way beyond generally linking the use of the judicial exception to a particular technological environment.

In particular, Claim 1 recites a matcher server including a processing system with at least one hardware processor, a memory, a FPGA circuit that comprises reconfigurable firmware logic circuitry and memory. Claim 8 recites a matcher server with a memory and a FPGA circuit. Claim 15 recites a FPGA circuit with a memory, a matcher server, reconfigurable firmware logic circuitry and memory. These elements are recited at a high level of generality (i.e., as a generic processor performing generic computer functions) such that that it amounts to no more than mere instructions to apply the exception using a generic computer component. Accordingly, these additional elements, when considered separately and as an ordered combination, do not integrate the abstract idea into a practical application because they do not impose any meaningful limits on practicing the abstract idea. Therefore, Claims 1, 8 and 15 are directed to an abstract idea without a practical application. (*Step 2A – Prong 2: No, the additional claimed elements are not integrated into a practical application)*

STEP 2B: If there is an exception, determine if the claim as a whole recites significantly more than the judicial exception itself.

The courts have recognized the following computer functions as well-understood, routine, and conventional functions when they are claimed in a merely generic manner (*e.g.,* at a high level of generality) or as insignificant extra-solution activity: i) receiving or transmitting data over a network, *e.g.,* using the Internet to gather data, *Symantec,* 838 F.3d at 1321, 120 USPQ2d at 1362 (utilizing an intermediary computer to forward information); *TLI Communications LLC v. AV Auto. LLC,* 823 F.3d 607, 610, 118 USPQ2d 1744, 1745 (Fed. Cir. 2016) (using a telephone for image transmission); *OIP Techs., Inc., v. Amazon.com, Inc.,* 788 F.3d 1359, 1363, 115 USPQ2d 1090, 1093 (Fed. Cir. 2015) (sending messages over a network); *buySAFE, Inc. v. Google, Inc.,* 765 F.3d 1350, 1355, 112 USPQ2d 1093, 1096 (Fed. Cir. 2014) (computer receives and sends information over a network); but see *DDR Holdings, LLC v. Hotels.com, L.P.,* 773 F.3d 1245, 1258, 113 USPQ2d 1097, 1106 (Fed. Cir. 2014) ("Unlike the claims in *Ultramercial,* the claims at issue here specify ***how*** interactions with the Internet are manipulated to yield a desired result--a result that overrides the routine and conventional sequence of events ordinarily triggered by the click of a hyperlink." (emphasis added)); ii) performing repetitive calculations, *Flook,* 437 U.S. at 594, 198 USPQ2d at 199 (recomputing or readjusting alarm limit values); *Bancorp Services v.*

Sun Life, 687 F.3d 1266, 1278, 103 USPQ2d 1425, 1433 (Fed. Cir. 2012) ("The computer required by some of *Bancorp*'s claims is employed only for its most basic function, the performance of repetitive calculations, and as such does not impose meaningful limits on the scope of those claims."); iii) electronic recordkeeping, *Alice Corp.,* 134 S. Ct. at 2359, 110 USPQ2d at 1984 (creating and maintaining "shadow accounts"); *Ultramercial,* 772 F.3d at 716, 112 USPQ2d at 1755 (updating an activity log); iv) storing and retrieving information in memory, *Versata Dev. Group, Inc. v. SAP Am., Inc.,* 793 F.3d 1306, 1334, 115 USPQ2d 1681, 1701 (Fed. Cir. 2015); *OIP Techs.,* 788 F.3d at 1363, 115 USPQ2d at 1092-93; v) electronically scanning or extracting data from a physical document, *Content Extraction and Transmission, LLC v. Wells Fargo Bank,* 776 F.3d 1343, 1348, 113 USPQ2d 1354, 1358 (Fed. Cir. 2014) (optical character recognition); and vi) a web browser's back and forward button functionality, *Internet Patent Corp. v. Active Network, Inc.,* 790 F.3d 1343, 1348, 115 USPQ2d 1414, 1418 (Fed. Cir. 2015). (MPEP §2106.05(d)(II))

This listing is not meant to imply that all computer functions are well-understood, routine, conventional activities, or that a claim reciting a generic computer component performing a generic computer function is necessarily ineligible. Courts have held computer-implemented processes not to be significantly more than an abstract idea (and thus ineligible) where the claim as a whole amounts to nothing more than generic computer functions merely used to implement an abstract idea, such as an idea that could be done by a human analog (i.e., by hand or by merely thinking). On the other hand, courts have held computer-implemented processes to be significantly more than an abstract idea (and thus eligible), where generic computer components are able in combination to perform functions that are not merely generic. (MPEP §2106.05(d)(II) – emphasis added)

Below are examples of other types of activity that the courts have found to be well-understood, routine, conventional activity when they are claimed in a merely generic manner (*e.g.,* at a high level of generality) or as insignificant extra-solution activity: recording a customer's order, *Apple, Inc. v. Ameranth, Inc.,* 842 F.3d 1229, 1244, 120 USPQ2d 1844, 1856 (Fed. Cir. 2016); shuffling and dealing a standard deck of cards, *In re Smith,* 815 F.3d 816, 819, 118 USPQ2d 1245, 1247 (Fed. Cir. 2016); restricting public access to media by requiring a consumer to view an advertisement, *Ultramercial, Inc. v. Hulu, LLC,* 772 F.3d 709, 716-17, 112 USPQ2d 1750, 1755-56 (Fed. Cir. 2014); identifying undeliverable mail items, decoding data on those mail items, and creating output data, *Return Mail, Inc. v. U.S. Postal Service,* -- F.3d --, -- USPQ2d --, slip op. at 32 (Fed. Cir. August 28, 2017); presenting offers and gathering statistics, *OIP Techs.,* 788 F.3d at 1362-63, 115 USPQ2d at 1092-93; determining an estimated outcome and setting a price, *OIP Techs.,* 788 F.3d at 1362-63, 115 USPQ2d at 1092-93; and arranging a hierarchy

of groups, sorting information, eliminating less restrictive pricing information and determining the price, *Versata Dev. Group, Inc. v. SAP Am., Inc.,* 793 F.3d 1306, 1331, 115 USPQ2d 1681, 1699 (Fed. Cir. 2015) (MPEP 2106.05(d))

Here, the steps are receiving or transmitting data over a network; performing repetitive calculations; storing and retrieving information in memory and electronically scanning or extracting data as well as setting or determining a price– all of which have been recognized by the courts as well-understood, routine and conventional functions.

The claims are directed to an abstract idea with additional generic computer elements that do not add meaningful limitations to the abstract idea because they require no more than a generic computer to perform generic computer functions that are well-understood, routine, and conventional activities previously known in the industry.

For the next step of the analysis, it must be determined whether the limitations present in the claims represent a patent-eligible application of the abstract idea. A claim directed to a judicial exception must be analyzed to determine whether the elements of the claim, considered both individually and as an ordered combination are sufficient to ensure that the claim as a whole amounts to significantly more than the exception itself.

For the role of a computer in a computer implemented invention to be deemed meaningful in the context of this analysis, it must involve more than performance of "well-understood, routine, [and] conventional activities previously known to the industry." Further, "the mere recitation of a generic computer cannot transform a patent ineligible abstract idea into a patent-eligible invention."

Applicant's specification discloses the following:

The specification notes that the exemplary system that is used to process orders and quotes uses a matcher server and interconnected trader servers, gateway servers, and market data servers. (See Applicant Specification paragraph 48 and Figure 2) None of these components are defined in the specification as being specialized or technological advancements, thus are assumed to be the servers and components generally found in financial exchange processing systems. In Figure 3, an example trading system shown in Figure 2 has a matcher server connected to a FPGA board. (See Applicant Specification paragraph 56 and Figure 3)

The detailed description describes various embodiments of the present invention for illustration purposes and embodiments of the present invention include the methods described and may be implemented using one or more apparatus, such as processing apparatus coupled to electronic media. Embodiments of the present invention may be stored on an electronic media (electronic memory, RAM,

ROM, EEPROM) or programmed as computer code (e.g., source code, object code or any suitable programming language) to be executed by one or more processors operating in conjunction with one or more electronic media storage. (See Applicant Specification paragraph 31)

Further, the specification discloses that "[a]lthough embodiments are described in terms of an FPGA, the embodiments are not limited to FPGAs but also include other integrated circuits such as ASIC that can be configured to process data as described herein." (See Applicant Specification paragraph 32)

Generic computer components recited as performing generic computer functions that are well-understood, routine and conventional activities amount to no more than implementing the abstract idea with a computerized system.

Looking at the limitations as an ordered combination adds nothing that is not already present when looking at the elements taken individually. There is no indication that the combination of elements improves the functioning of a computer or improves any other technology. The collective functions appear to be implemented using conventional computer systemization.

The claim(s) does/do not include additional elements that are sufficient to amount to significantly more than the judicial exception. Upon reconsideration of the indicia noted under Step 2A in concert with the Step 2B considerations, the additional claim element(s) amounts to no more than mere instructions to apply the exception using generic computer components. The same analysis applies in Step 2B, i.e., mere instructions to apply an exception using a generic computer component cannot integrate a judicial exception into a practical application at Step 2A or provide an inventive concept in Step 2B. The claim does not provide an inventive concept significantly more than the abstract idea.

Accordingly, these additional elements, when considered separately and as an ordered combination, do not integrate the abstract idea into a practical application because they do not impose any meaningful limits on practicing the abstract idea.

The independent claims 1, 8 and 15 are not patent eligible. (St*ep 2B: NO. The claims do not provide significantly more*)

Dependent Claims 2-7, 9-14 and 16-20 further define the abstract idea that is presented in the respective **independent Claims 1, 8 and 15** and are further grouped as certain methods of organizing human activity and are abstract for the same reasons and basis as presented above. No additional hardware components other than those found in the respective independent claims is recited, thus it is presumed that the claim is further utilizing the same generic systemization as presented above. The dependent claims do not include any additional elements that integrate the abstract idea into a practical

application of the exception or are sufficient to amount to significantly more than the judicial exception when considered both individually and as an ordered combination.

Therefore, the dependent claims are also directed to an abstract idea.

Thus, **Claims 1-20** are rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter.

Regarding Claims 15-20, these claims are further rejected as the claimed invention is directed to non-statutory subject matter. The claim(s) does not fall within at least one of the four categories of patent eligible subject matter because a FPGA circuit is not one of the four categories of patent eligible subject matter.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 15-20** are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Regarding Claim 15, the preamble has a number of structural pieces and functions that are recited in the preamble, but that are not necessarily recited in the claim itself, leading Examiner to question which elements are actually in the claim and which elements are not part of the claim. **Dependent Claims 16-20** are further rejected on the basis of a rejected base claim.

Relevant Prior Art

The following prior art is considered to be relevant to the instant application, but is currently not being applied.

Taylor et al. (US PG Pub. 2012/0095893) – *disclosing embodiments for hardware accelerating the processing of financial market depth.*

Jimenez et al. (US PG Pub. 2008/0133395) – *disclosing an efficient data dissemination method and system in an active market environment.*

Taylor et al (US PG Pub. 2009/0182683) – *disclosing a basket calculation engine to receive a stream of data and accelerate the computation of basket values based on that data where the coprocessor is a FPGA.*

Response to Arguments

Applicant's arguments filed June 19, 2020 have been fully considered but they are not fully persuasive as disclosed below.

As to the Claim Objections:

Applicant's amendments have obviated the objections.

As to the 112 Rejections:

Applicant's amendments resolved some of the 112 rejections as noted above.

As to the 101 Rejection:

Examiner acknowledges Applicant's argument, however is of another opinion. While Applicant wishes to argue the benefits of how the messages are handled, the claims do not reflect the improvement Applicant is arguing. The limitations being claimed are abstract as noted above in the rejection in chief.

As to Prong 2 of Step 2A, the same problem persists. While the specification notes the need to increase capacity, the claims do not reflect an improved capacity or disclose how latency would be improved. The claims are not similar to those seen in Example 40 as the claims at issue in the example disclose a specific improvement. The claims in the instant application do not.

As to Step 2B, the underlying issue remains the same. The claims themselves do not reflect the alleged improvements that Applicant is arguing. Examiner cannot import the specification into the claims.

The 101 Rejection is maintained.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AMBREEN A ALLADIN whose telephone number is (571)270-3533. The examiner can normally be reached on Monday - Friday 9-5.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shahid R. Merchant can be reached on 571-270-01360. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/AAA/
July 5, 2020

/Jason Borlinghaus/
Primary Examiner, Art Unit 3693
July 6, 2020

REMARKS

Entry, reconsideration, and allowance are respectfully requested.

Interview

During a telephone interview with the Examiner and the undersigned conducted on September 14, 2020, the Examiner suggested canceling claims 15-20 and proceeding with an after final response arguing the patent eligibility for claims 1-14. By this amendment, claims 15-20 are canceled without prejudice to pursing their prosecution in a continuation application. This renders moot the rejections of claim 15-20 under 35 U.S.C. §101 and 35 U.S.C. §112(b). Claims 1-14 are patent eligible for at least the reasons set forth below.

Patent Eligibility

The sole remaining rejection in this case is that of claims 1-14 rejected under 35 U.S.C. §101. This rejection is respectfully traversed.

Step 2A

Prong One

Page 3 of the final office action (FOA) states: "The series of steps recited describe using a distributed computing to receive orders, send orders, parse orders, match orders, update data and deliver information regarding the match which is a fundamental economic practice and a commercial or legal interaction and thus grouped as certain methods of organizing human activity which is an abstract idea." Applicant disagrees.

In *Data Engine Technologies LLC v. Google LLC*, 906 F.3d 999 (Fed. Cir. 2018), the Court reminded the parties:

> At *Alice* step one, "it is not enough to merely identify a patent-ineligible concept underlying the claim; we must determine whether that patent-ineligible concept is what the claim is 'directed to.'" [cite omitted] And that inquiry requires that the claims be read as a whole.

Data Engine, 906 F.3d at 1011. The court went on to say that "Representative claim 12 recites precisely this technical solution and improvement in computer spreadsheet functionality. The claim recites specific steps detailing the method of navigating through spreadsheet pages within a three-dimensional spreadsheet environment using notebook tabs." *Data Engine,* 906 F.3d at 1008.

The claims are directed to computer technology. Claim 1 defines a "distributed computer system for handling electronic data messages," and claim 8 is a corresponding "method for handling electronic data messages in a distributed computer system." The focus of claims 1 and 8 is not matching, a fundamental economic practice, a commercial or legal interaction, or organizing human activity. Instead, the claimed technology is directed to solving data processing latency/delay problems when handling electronic messages and improving the speed by which those electronic messages are processed. See, e.g., [0041] of the specification. Processing latency/delay is a *technical* problem. Overloading a matching server with processing large amounts of electronic messages is another technical problem. See, e.g., [0050] of the specification. Paragraph [0040] identifies a "growing and significant need to improve the capacity and reduce the latency" of complex computer trading exchanges. Paragraph [0039] describe hardware and paragraph [0058] refers to a process in the specification that reduces latency and increases capacity.

The claimed technology solves these technical problems and improves data processing efficiency and speed as a result of the specific way in which the distributed components are organized. Claims 1 and 8 do not simply recite "generic" components to perform generic functions. Rather, claim 1 recites a matcher server, a gateway, and an FPGA circuit that are configured in specific ways to perform non-generic operations. For example, the gateway, in addition to routing order electronic messages directly to the matcher server for matching processing, also routes mass quote electronic messages to the FPGA circuit *without first involving the matcher server*. The FPGA *parses each individual message* of the mass quote electronic message and stores data for each one to a *data structure* located in the memory of the FPGA. The claims specify that the data structure is organized according to both an instrument identifier of a corresponding electronic message and a first client identifier that corresponds to the first client that sent the first mass quote electronic message. The FPGA also updates that data structure based on reception of specific "away market feed" electronic messages. The FPGA responds to a particular type of query which is sent as part of the matching process performed on the matcher server for the first instrument to deliver information from the data structure regarding the first instrument. That information delivered is particular (not generic) and includes data based on away market feed electronic messages for the first instrument and data based on

individual quote electronic messages for the first instrument that were part of at least one received mass quote electronic message.

Because claims 1 and 8 provide technical solutions to technical problems confronting complex computerized trading exchanges and a technical improvement to existing computerized trading exchanges, under prong one of Step 2A, the claims are not directed to an abstract idea and are patent eligible.

Prong 2

The claims are also patent eligible under prong two of Step 2A because they recite specifically-configured electronic components that distributively cooperate to solve the technical problems identified above and in the specification and to improve operation of the distributed computer system. The specification at [0011] provides an example illustrating a technical problem at the time of filing addressed by the claimed technology:

> For instance, the International Stock Exchange (ISE) at present trades 500,000 different instruments--and this number grows over time. Many market makers submit firm quotes for all 500,000 instruments. To maintain accurate prices for all their quotes, market makers *need to be able to update their quotes quickly*. ISE provides market makers with special mass quote functions that allow them to update their quotes in many instruments in a single message. *The number of Mass Quote messages that can be processed by ISE is limited by the speed of the servers and networks.* For example, at present, ISE will accept up to 40,000 Mass Quote update messages from a single market maker in a single second. But when the stock market moves quickly, even this large *capacity is not sufficient* for the market makers to move all their quotes in all instruments.

Paragraph [0012] explains that "each market maker must update thousands of instruments any times per second."

Then, specification paragraph [0039] describes some technical advantages of the claimed technology including "*increased capacity* of exchanges by using an FPGA device to process certain messages." This paragraph reiterates several technical problems with conventional exchanges, i.e., "*Conventional exchanges lack the capacity to execute and process the millions of messages sent to the exchange each second. Conventional exchanges also need to increase their capacity* to read messages sent to the exchange while also delivering market data feeds to clients." Specification paragraph [0040] then identifies "a growing and significant *need to*

improve the capacity and reduce the latency." Paragraph [0041] explains prior attempt to adjust for the capacity limitations including setting limits for the throughput to keep the servers "lightly loaded." But this server "throttling" results in "queues of messages waiting to be processed. This poses a problem as it increases the latency."

Paragraph [0043] of the specification describes another technical advantage where the matcher server can perform more complex functions having offloaded the time consuming message handling to the FPGA. [0044] states "[a]nother exemplary advantage of embodiments of the disclosed trading system is the ability to inform users as to the state of their quote with *greater accuracy*." Specification paragraph [0057] describes the increased processing speed achieved, and specification paragraph [0058] again highlights the reduced overall latency on the system.

The *2019 Revised Patent Subject Matter Eligibility Guidance (PEG)* Example 40 focuses on a claim reciting:

> collecting, by the network appliance, traffic data relating to the network traffic passing through the network appliance, the traffic data comprising at least one of network delay, packet loss, or jitter;
>
> comparing, by the network appliance, at least one of the collected traffic data to a predefined threshold; and
>
> collecting additional traffic data relating to the network traffic when the collected traffic data is greater than the predefined threshold, the additional traffic data comprising Netflow protocol data.

The Example 40 claim recites collecting network data, comparing it (matching) to a threshold, and collecting more data when the threshold is exceeded. The *PEG* found a practical application because "the method limits collection of additional Netflow protocol data to when the initially collected data reflects an abnormal condition, which *avoids excess traffic volume on the network and hindrance of network performance ... This provides a specific improvement over prior systems,* resulting in improved network monitoring" (emphasis added). In other words, the practical application was identifying and matching collected network data to *take an action to reduce excess traffic volume*.

Page 10 of the FOA argues "[t]he claims are not similar to those seen in Example 40 as the claims at issue in the example disclose a specific improvement. The claims in the instant

application do not." Applicant disagrees. The claim in example 40 recites "collecting additional traffic data relating to the network traffic when the collected traffic data is greater than the predefined threshold, the additional traffic data comprising Netflow protocol data." This is no more of "a specific improvement" than the following text from claim 1:

> [the gateway] route[s] the mass quote electronic message to a field programmable gate array (FPGA) circuit *without first involving the matcher server*; and
>
> the *field programmable gate array (FPGA) circuit* that comprises reconfigurable firmware logic circuitry and memory located on the FPGA circuit, the reconfigurable firmware logic circuitry configured to:
>
> receive the mass quote electronic message routed from the gateway,
>
> parse each one of the plurality of individual quote electronic messages of the mass quote electronic message and store data for each one of the plurality of individual quote electronic messages to a data structure located in the memory of the FPGA, where the data stored for each one of the plurality of individual quote electronic messages is organized in the data structure according to both the instrument identifier of a corresponding electronic message and a first client identifier that corresponds to the first client that sent the first mass quote electronic message,
>
> receive away market feed electronic messages from remotely located exchange computer systems, where each of the away market feed electronic messages includes a price value and a corresponding instrument identifier and each of the away market feed electronic messages are received by the FPGA *without first being routed through the matcher server or the gateway*,
>
> *update the data structure* based on reception of the away market feed electronic messages, and
>
> *deliver, in response to a query sent as part of the matching process performed on the matcher server* for the first instrument, *information stored in the data structure* regarding the first instrument, the delivered information including data based on away market feed electronic messages for the first instrument and data based on individual quote electronic messages for the first instrument that were part of at least one received mass quote electronic message.

Like the "collecting additional traffic data relating to the network traffic when the collected traffic data is greater than the predefined threshold" in Example 40, claim 1 handles "additional information" of a different type, i.e., mass quote message, differently from individual order electronic messages. Rather than routing a first order electronic message directly to the matcher server for the matching process, the gateway detects "additional information" and routes the mass quote messages to the FPGA for processing rather than to the matching server.

The technology recited in claims 1 and 8 has a similar practical application as the claim in Example 40 because it provides a specific technical improvement over conventional computerized exchanges in terms of *reducing network and processing latency* and *improving the accuracy and speed (improved performance) of the exchange network*. The similarity between this and Example 40 is striking and compels that claims 1-14 be found patent eligible just like the claim in Example 40.

The *PEG* further states "an additional element [that] reflects an improvement in the functioning of a computer, or an improvement to other technology or technical field" is "indicative that an additional element (or combination of elements) may have integrated the exception into a practical application." See page 19. "Examiners should note, however, that revised Step 2A specifically *excludes consideration of whether the additional elements represent well-understood, routine, conventional activity*...Accordingly, in revised Step 2A examiners should ensure that they give weight to all additional elements, whether or not they are conventional, when evaluating whether a judicial exception has been integrated into a practical application." See *PEG* page 19 (emphasis added). The FOA's prong 2 analysis improperly relies on dismissive statements like "a generic processor performing generic computer functions."

In addition, the claimed computer components in the claims are specifically configured to perform or carry out specific functions that are non-generic, and therefore, the claimed computer elements are not generic.

For the reasons just explained, the claims are not directed to an abstract idea under prong two of Step 2A and are patent eligible.

Step 2B

Page 7 of the FOA asserts:

> Here, the steps are receiving or transmitting data over a network; performing repetitive calculations; storing and retrieving information in memory and electronically scanning or extracting data as well as setting or determining a price- all of which have been recognized by the courts as well understood, routine and conventional functions.
>
> The claims are directed to an abstract idea with additional generic computer elements that do not add meaningful limitations to the abstract idea because they require no more than a generic computer to perform generic computer functions that are well-understood, routine, and conventional activities previously known in the industry.

Nothing in this text relates to the *specific language* recited in the independent claims *read as a whole*. When read as a whole, each of claims 1 and 8 recites an "ordered combination of limitations" that transforms any abstract idea "into a particular, practical application of that abstract idea." See *BASCOM Glob. Internet Servs., Inc.* v. *AT&T Mobility LLC*, 827 F.3d 1341, 1352 (Fed. Cir. 2016) (finding claims eligible if the ordered combination of claim limitations "transform[s] the abstract idea . . . into a particular, practical application of that abstract idea.")

The statement on page 8 of the OA, "In Figure 3, an example trading system shown in Figure 2 has a matcher server connected to a FPGA board," ignores the bulk of the language in the independent claims. The ordered combination of features in claim 1 recites specific ways in which the matcher server is configured, the gateway is configured, and the FPGA is configured to function and interact in ways that matcher servers, gateways, and FPGAs in conventional exchanges do not.

Page 8 of the FOA concludes with "there is no indication that the combination of elements improves the functioning of a computer or improves any other technology." This is simply not correct. As explained above and throughout the specification, see the example references to the specification identified in the Step 2A prong 1 and 2 analyses above, **the specific combination of features recited in independent claims 1 and 8 does in fact improve over conventional computer exchanges in terms of reduced latency, improved accuracy, and improved speed of operation**. Therefore, claims 1 and 8 do recite a particular, practical application of any abstract idea.

In addition, the claims in this application are like those in *BASCOM* where the court identified *the distributed nature* of the filtering system as an "inventive" concept for purposes of step two. The instant claims specifically recite a "distributed computer system," and the "distributed nature" of claim 1 is quite evident with the claimed matcher server, the memory, the remote client computer system, and the field programmable gate array (FPGA) circuit. Furthermore, the claims set forth specific technical features that explain in greater detail how the distributed components interact with each other.

Accordingly, under Step 2B, the claims are not directed to an abstract idea and are patent eligible.

The claims are statutory under each of Step 2A, prong 1, Step 2A, prong 2, and Step 2B. The rejection under 35 U.S.C. §101 should be withdrawn.

The application is in condition for allowance. An early notice to that effect is requested.

The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to Deposit Account No. 14-1140.

Respectfully submitted,

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AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A distributed computer system for handling electronic data messages, the distributed computer system comprising:

a matcher server configured to store, in memory, an order book that stores pending orders, the matcher server including a processing system with at least one hardware processor, the processing system configured to:

receive a first order electronic message for a first instrument, and

in response to reception of the first order electronic message, perform a matching process based on the first order electronic message;

a gateway configured to:

receive the first order electronic message and route the first order electronic message directly to the matcher server for the matching process,

receive a first mass quote electronic message from a remote client computer system that is associated with a first client, the first mass quote electronic message including a plurality of individual quote electronic messages that are bundled into the first mass quote electronic message, each one of the plurality of individual quote electronic messages including a price value for one of a plurality of different instrument identifiers included with a respective one of the plurality of individual quote electronic messages,

route the mass quote electronic message to a field programmable gate array (FPGA) circuit without first involving the matcher server; and

the field programmable gate array (FPGA) circuit that comprises reconfigurable firmware logic circuitry and memory located on the FPGA circuit, the reconfigurable firmware logic circuitry configured to:

receive the mass quote electronic message routed from the gateway,

parse each one of the plurality of individual quote electronic messages of the mass quote electronic message and store data for each one of the plurality of individual quote electronic messages to a data structure located in the memory of the FPGA, where the data stored for each one of the plurality of individual quote electronic messages is organized in the data

structure according to both the instrument identifier of a corresponding electronic message and a first client identifier that corresponds to the first client that sent the first mass quote electronic message,

receive away market feed electronic messages from remotely located exchange computer systems, where each of the away market feed electronic messages includes a price value and a corresponding instrument identifier and each of the away market feed electronic messages are received by the FPGA without first being routed through the matcher server or the gateway,

update the data structure based on reception of the away market feed electronic messages, and

deliver, in response to a query sent as part of the matching process performed on the matcher server for the first instrument, information stored in the data structure regarding the first instrument, the delivered information including data based on away market feed electronic messages for the first instrument and data based on individual quote electronic messages for the first instrument that were part of at least one received mass quote electronic message.

2. (Original) The distributed computer system of claim 1,

wherein update of the data structure based on reception of the away market feed electronic messages further includes: update of a most recent price value for a corresponding instrument identifier along with an exchange code.

3. (Previously Presented) The distributed computer system of claim 1, wherein the reconfigurable firmware logic circuitry is further configured to:

receive, from the matcher server, a match message; and

in response to reception of the match message, update the data structure, generate and transmit a market data feed update electronic message to remote computer systems.

4. (Original) The distributed computer system of claim 1, wherein the matcher server uses the most recent information for an instrument to determine if an order for that corresponding instrument has been processed.

5. (Previously Presented) The distributed computer system of claim 1, wherein the reconfigurable firmware logic circuitry is further configured to:

determine one of the parsed plurality of individual quote messages is matchable against another quote and/or an order in the order book,

in response to the determination, generate and send a match-related message to the gateway, where the gateway is further configured to route the match-related message to the matcher server for processing.

6. (Original) The distributed computer system of claim 1, wherein the reconfigurable firmware logic circuitry is further configured to:

send, in response to reception of the mass quote electronic message, at least one acknowledgement electronic message, wherein each acknowledgement electronic message includes a sequencer number that corresponds to a logical processing order for a corresponding quote.

7. (Previously Presented) The distributed computer system of claim 1, wherein the away market feed electronic messages include trading state messages, and wherein the reconfigurable firmware logic circuitry is further configured to:

determine that the trading state of an underlying market has changed in response to reception of a trading state message; and

in response to the determination, send a notice message to the matcher server relating to contents of the trading state message.

8. (Original) A method for handling electronic data messages in a distributed computer system, the method comprising:

storing in memory, by a matcher server, an order book that stores pending orders;

receiving by the matcher server a first order electronic message for a first instrument;

in response to reception of the first order electronic message, the matcher server performing a matching process based on the first order electronic message;

receiving by a gateway the first order electronic message and route the first order electronic message directly to the matcher server for the matching process;

receiving by the gateway a first mass quote electronic message from a remote client computer system that is associated with a first client, the first mass quote electronic message including a plurality of individual quote electronic messages that are bundled into the first mass quote electronic message, each one of the plurality of individual quote electronic messages including a price value for one of a plurality of different instrument identifiers included with a respective one of the plurality of individual quote electronic messages;

routing by the gateway the mass quote electronic message to a field programmable gate array (FPGA) circuit without first involving the matcher server;

receiving by the FPGA the mass quote electronic message routed from the gateway;

parsing by the FPGA each one of the plurality of individual quote electronic messages of the mass quote electronic message and store data for each one of the plurality of individual quote electronic messages to a data structure located in the memory of the FPGA, where the data stored for each one of the plurality of individual quote electronic messages is organized in the data structure according to both the instrument identifier of a corresponding electronic message and a first client identifier that corresponds to the first client that sent the first mass quote electronic message;

receiving by the FPGA away market feed electronic messages from remotely located exchange computer systems, where each of the away market feed electronic messages includes a price value and a corresponding instrument identifier and each of the away market feed electronic messages are received by the FPGA without first being routed through the matcher server or the gateway;

updating by the FPGA the data structure based on reception of the away market feed electronic messages; and

delivering by the FPGA, in response to a query sent as part of the matching process performed on the matcher server for the first instrument, information stored in the data structure regarding the first instrument, the delivered information including data based on away market feed electronic messages for the first instrument and data based on individual quote electronic messages for the first instrument that were part of at least one received mass quote electronic message.

9. (Original) The method of claim 8, wherein update of the data structure based on reception of the away market feed electronic messages further includes: update of a most recent price value for a corresponding instrument identifier along with an exchange code.

10. (Previously Presented) The method of claim 8, further comprising:

receiving by the FPGA, from the matcher server, a match message; and

in response to reception of the match message, updating by the FPGA the data structure, generate and transmit a market data feed update electronic message to remote computer systems.

11. (Original) The method of claim 8, further comprising the matcher server using the most recent information for an instrument to determine if an order for that corresponding instrument has been processed.

12. (Previously Presented) The method of claim 8, further comprising:

determining by the FPGA that one of the parsed plurality of individual quote messages is matchable against another quote and/or an order in the order book,

in response to the determining, generating and sending by the FPGA a match-related message to the gateway, where the gateway is further configured to route the match-related message to the matcher server for processing.

13. (Original) The method of claim 8, further comprising sending by the FPGA, in response to reception of the mass quote electronic message, at least one acknowledgement electronic message, wherein each acknowledgement electronic message includes a sequencer number that corresponds to a logical processing order for a corresponding quote.

14. (Original) The method of claim 8, wherein the away market feed electronic messages include trading state messages, and the FPGA further:

determining that the trading state of an underlying market has changed in response to reception of a trading state message; and

in response to the determination, sending a notice message to the matcher server relating to contents of the trading state message.

15-20. Canceled.